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Abstract: The integrity of gate oxides formed on the device surfaces of SIMOX wafers has been a concern because of the structural imperfection of SIMOX superficial **silicon** layers compared to bulk **silicon** and the potential for metal contamination during the extended oxygen implantation. Although procedures for improving the crystalline perfection of the surface layer have been developed, and steps taken by oxygen implanter modification and introduction of TCA into the anneal ambient to reduce sources of metal contamination, the concern has remained because of the relative newness of the technology and the limited oxide integrity data presented for SIMOX structures so far. In this paper, we present results of ramp voltage breakdown and constant current charge to breakdown measurements on 6 and 20 nm gate oxides formed on SIMOX surfaces prepared by standard cycle SIMOX **annealing** in ambients containing various **halogen** levels, and variations in implantation screen oxide presence and thickness. This latter variation was done by processing 'standard SIMOX' material without screen oxide, and forming a tapered screen oxide on a second SIMOX batch by gradual immersion oxide etching. The tapered screen oxide has been found to provide spatially controlled variation in SIMOX dislocation density for correlation with the electrical parameters. Homogeneous bulk **silicon** wafers were used as controls in all the SIMOX anneal process variations, and un-annealed bulk control wafers were also included. Atomic force microscopy (AFM) was used to measure surface **roughness** for correlation with the process variables. (0 Refs)
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INTEGRITY OF GATE OXIDES FORMED ON SIMOX WAFERS

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Introduction

The integrity of gate oxides formed on the device surfaces of SIMOX wafers has been a concern because of the structural imperfection of SIMOX superficial silicon layers compared to bulk silicon and the potential for metal contamination during the extended oxygen implantation. Although procedures for improving the crystalline perfection of the surface layer have been developed, and steps taken by oxygen implanter modification and introduction of TCA into the anneal ambient to reduce sources of metal contamination, the concern has remained because of the relative newness of the technology and the limited oxide integrity data presented for SIMOX structures so far.

In this paper, we present results of ramp voltage breakdown and constant current charge to breakdown measurements on 6 and 20 nm gate oxides formed on SIMOX surfaces prepared by standard cycle SIMOX annealing in ambients containing various halogen levels, and variations in implantation screen oxide presence and thickness. This latter variation was done by processing 'standard SIMOX' material without screen oxide, and forming a tapered screen oxide on a second SIMOX batch by gradual immersion oxide etching. The tapered screen oxide has been found to provide spatially controlled variation in SIMOX dislocation density for correlation with the electrical parameters. Homogeneous bulk silicon wafers were used as controls in all the SIMOX anneal process variations, and un-annealed bulk control wafers were also included. Atomic force microscopy (AFM) was used to measure surface roughness for correlation with the process variables, all of which will be discussed in the presentation.

Experimental Details

The MOS capacitors used in this study were built on n-type single-implanted (dose = 1.80×10^{18} O^+/cm^2) SIMOX and bulk wafers, using a multiple area capacitor array with a polysilicon gate process in which the superficial silicon surrounding the capacitor was doped simultaneously with the gate electrode, providing a top surface contact for the capacitor channel region. Gate oxides were grown in an O_2- 5% HCl ambient.

Ramp voltage breakdown (RVB) measurements were made on large area (0.02 cm^2) capacitors, with breakdown defined as passage of 100 mA/cm^2. The charge to breakdown (Q_{bd}) measurements were done on smaller (0.0002 cm^2) capacitors, which should be largely unaffected by the gross defects found in the RVB tests. Fowler-Nordheim stress current density was +100 mA/cm^2. All electrical measurements were made with positive bias on the gate, accumulating the channel region to enhance its electrical contact. This polarity causes electron injection into the oxide from the superficial silicon-gate oxide interface, the interface of primary concern here.

Results

Acceptable values of breakdown voltage and Q_{bd} were found for all standard SIMOX groups. Improved Q_{bd} distributions were found for decreasing HCl (or TCA), as shown in Figure 1, which may correlate with increase surface roughness. This pattern was not reproduced in the breakdown voltage data of Figure 2. However, this correlation is not necessarily expected since the "no TCA" sample may have degradation from metallic impurities. A stronger and consistent dependence on material preparation is found in the data comparing the standard SIMOX, tapered screen oxide SIMOX, and bulk silicon materials. Although some samples from each of the three materials groups reached the same high values of breakdown voltage and Q_{bd} for both oxide thicknesses, the tapered screen oxide group displayed the highest defect density. This is illustrated in Figures 3 and 4, Q_{bd} distributions for the 20 and 6 nm oxides grouped by material type, with all TCA variations merged. Primary mode Q_{bd} values of 45 C/cm^2 for the 20 nm films and 150 C/cm^2 for the 6 nm oxides indicate a reasonable level of process cleanliness for the overall experiment. In the screen oxide thickness study, the screen oxide was tapered from no oxide at the wafer flat to 250 nm at the top, and Q_{bd} measurements were made at nine equally spaced locations normal to the thickness variation. A region near the flat where the screen oxide was 30-60 nm thick consistently gave very low Q_{bd}, while other sites gave scattered results, as shown in Figure 5. This region near the flat was found to be the site of highest dislocation density.

Conclusions

While this data indicates that more work needs to be done to improve SIMOX surface quality and to optimize its processing, the low levels of gross defects found here, the fact that the SIMOX samples matched maximum BV and Q_{bd} values with the bulk silicon samples, and the high percentage of Q_{bd} values above 1 C/cm^2 suggest that current standard SIMOX material is adequate for processing today's complex SOI CMOS circuits.

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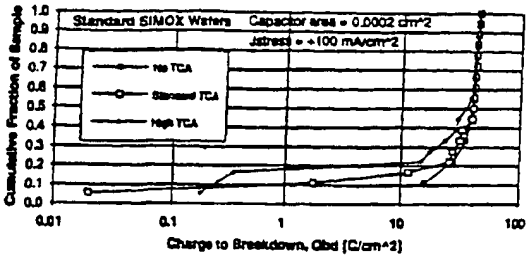

Figure 1. Charge to breakdown, Q_{bd}, for 20 nm gate oxides on standard SIMOX wafers as a function of TCA level.

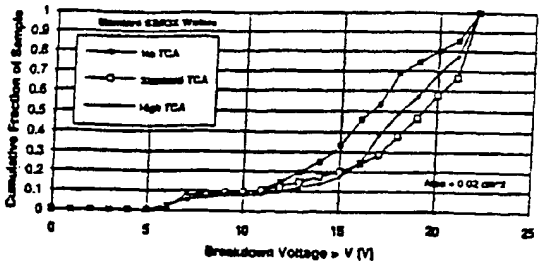

Figure 2. Ramp voltage breakdown as a function of TCA level for the wafers of Fig. 1.

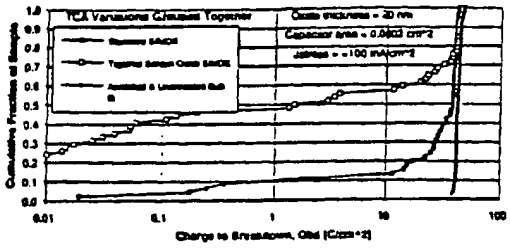

Figure 3. Charge to breakdown as a function of material type for the 20 nm oxides, with TCA level variations merged.

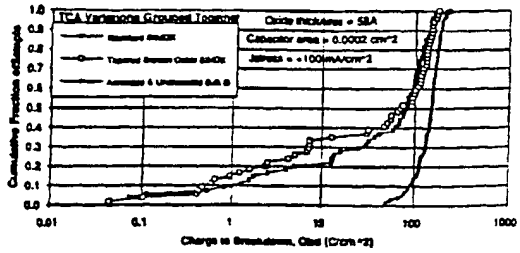

Figure 4. Charge to breakdown as a function of material type for the 6 nm oxides, with TCA level variations merged.

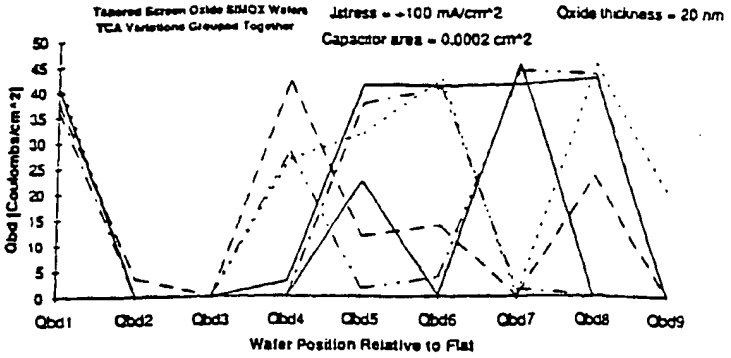

Figure 5. Spatial variation of Q_{bd} on tapered screen oxide SIMOX wafers, normal to thickness gradient. Measurement positions Qbd2 and Qbd3 correspond to screen oxide thicknesses between 30-60 nm, the region of highest SIMOX surface dislocation density.